

FIG. 1

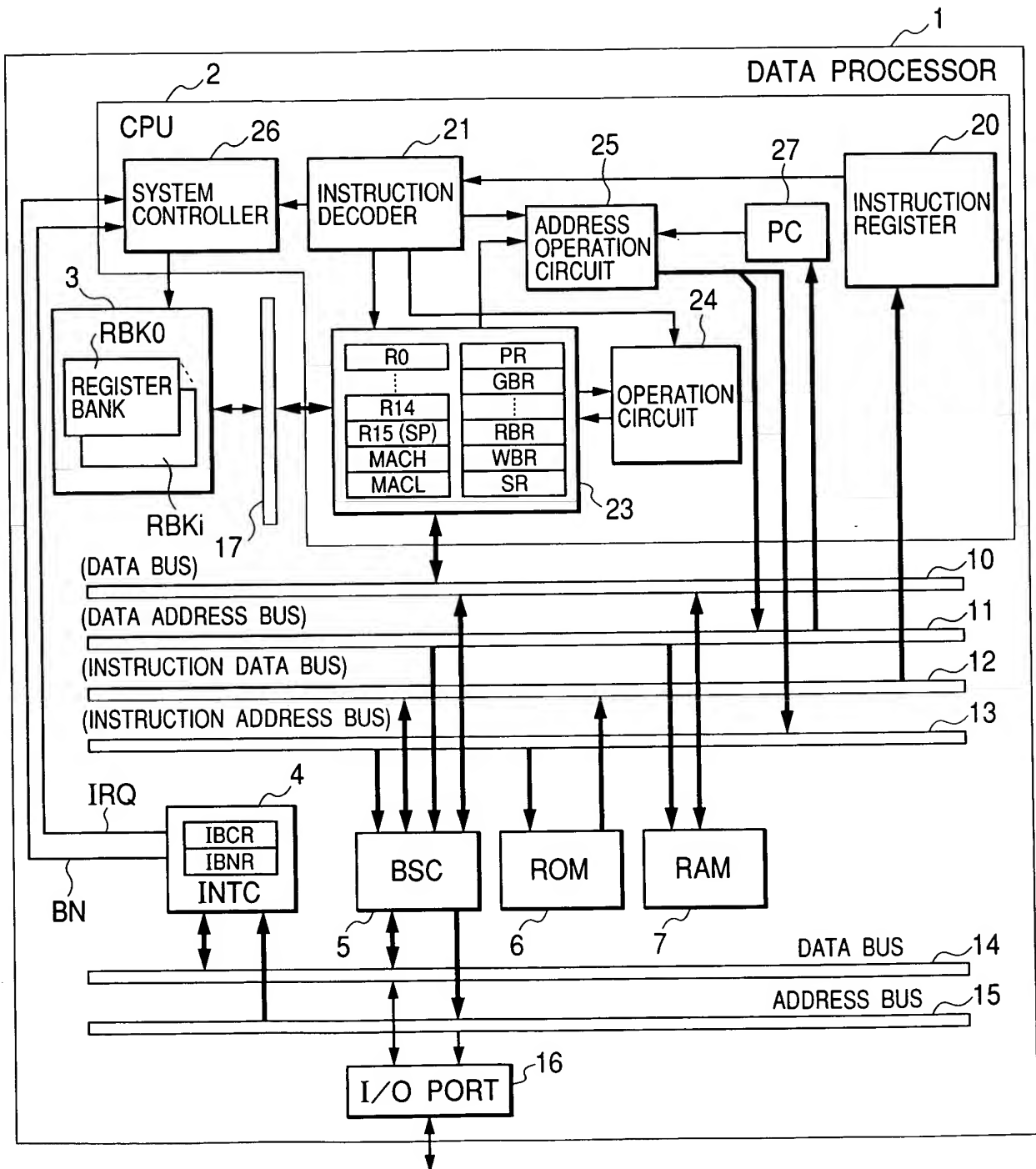


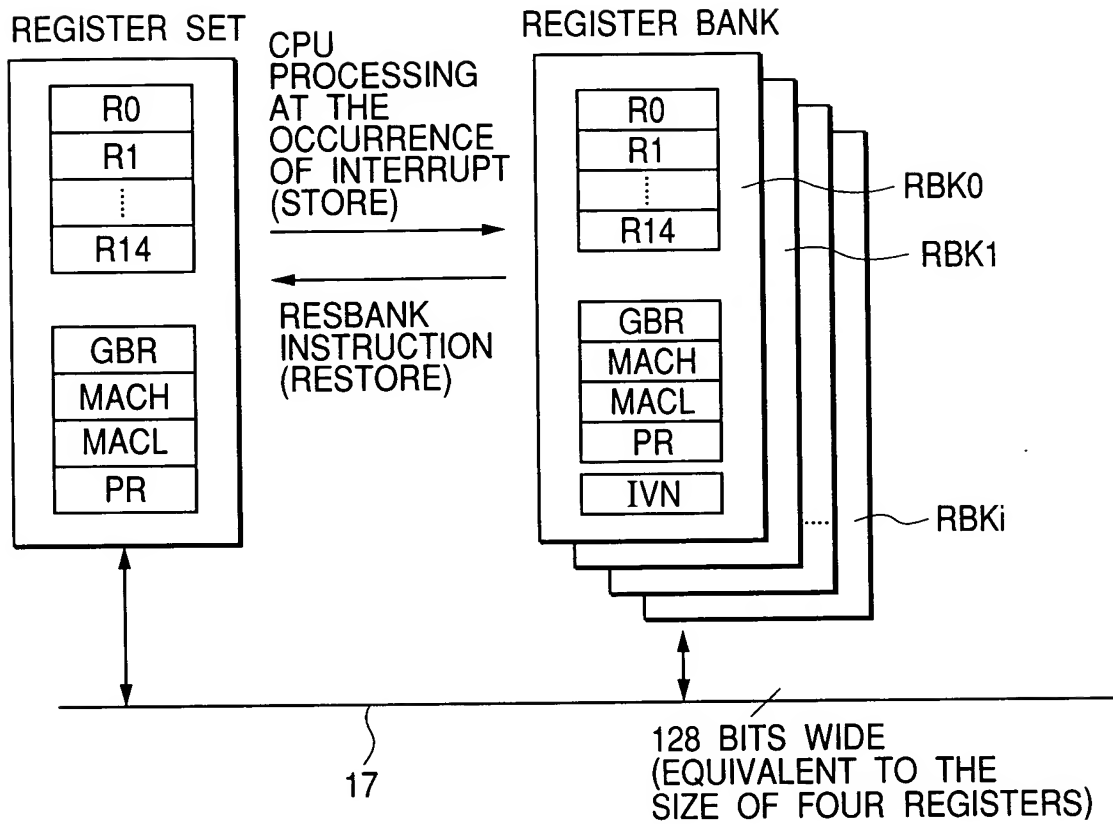
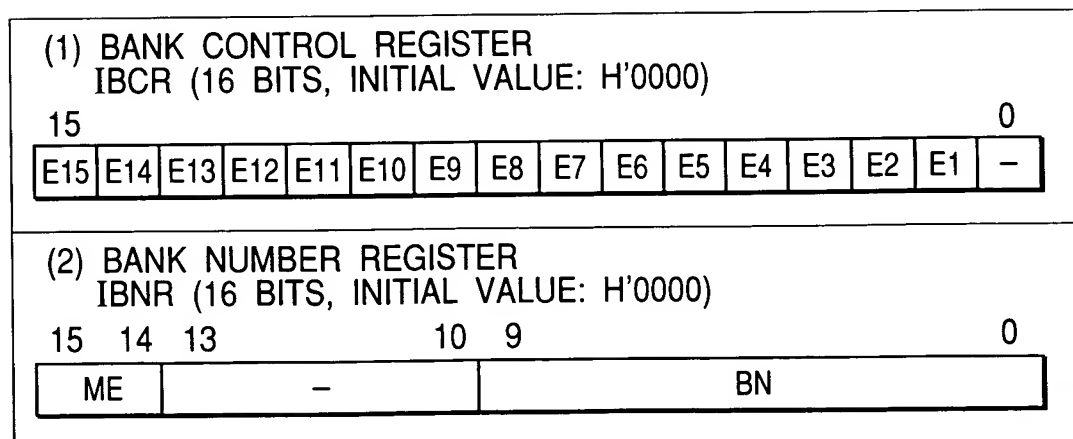
FIG. 2**FIG. 3**

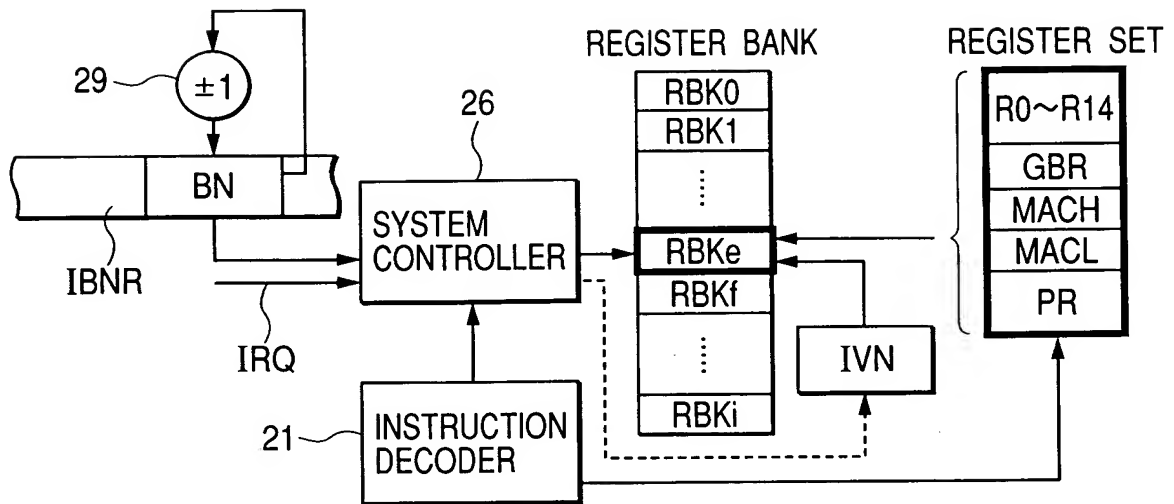
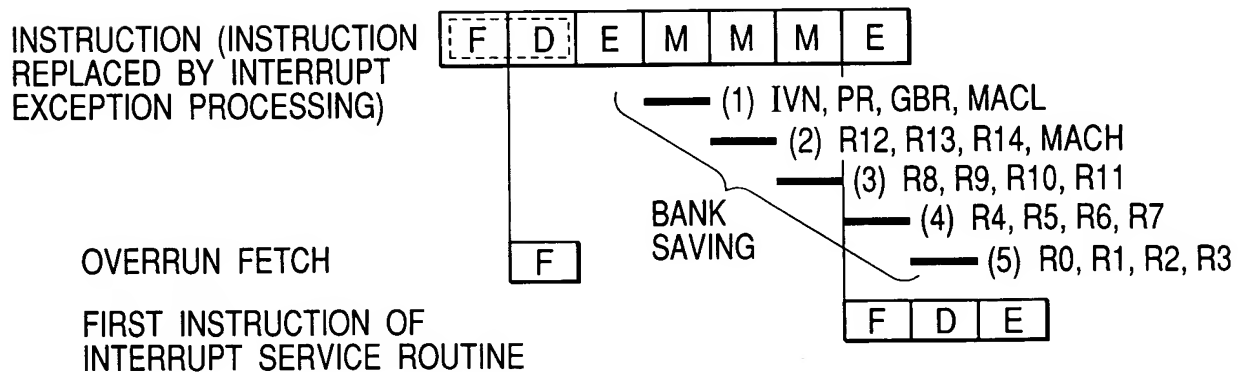
FIG. 4**FIG. 5**

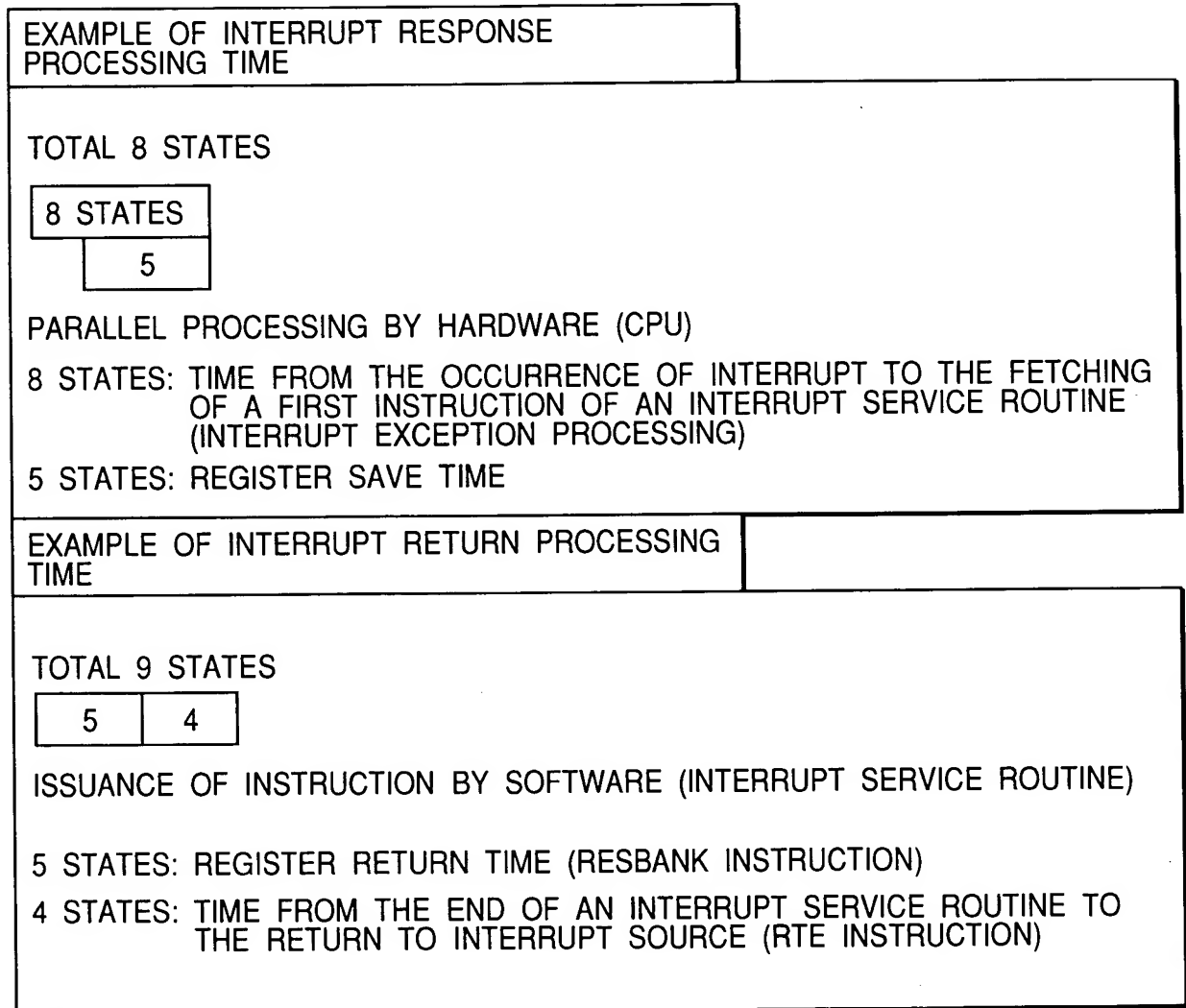
FIG. 6

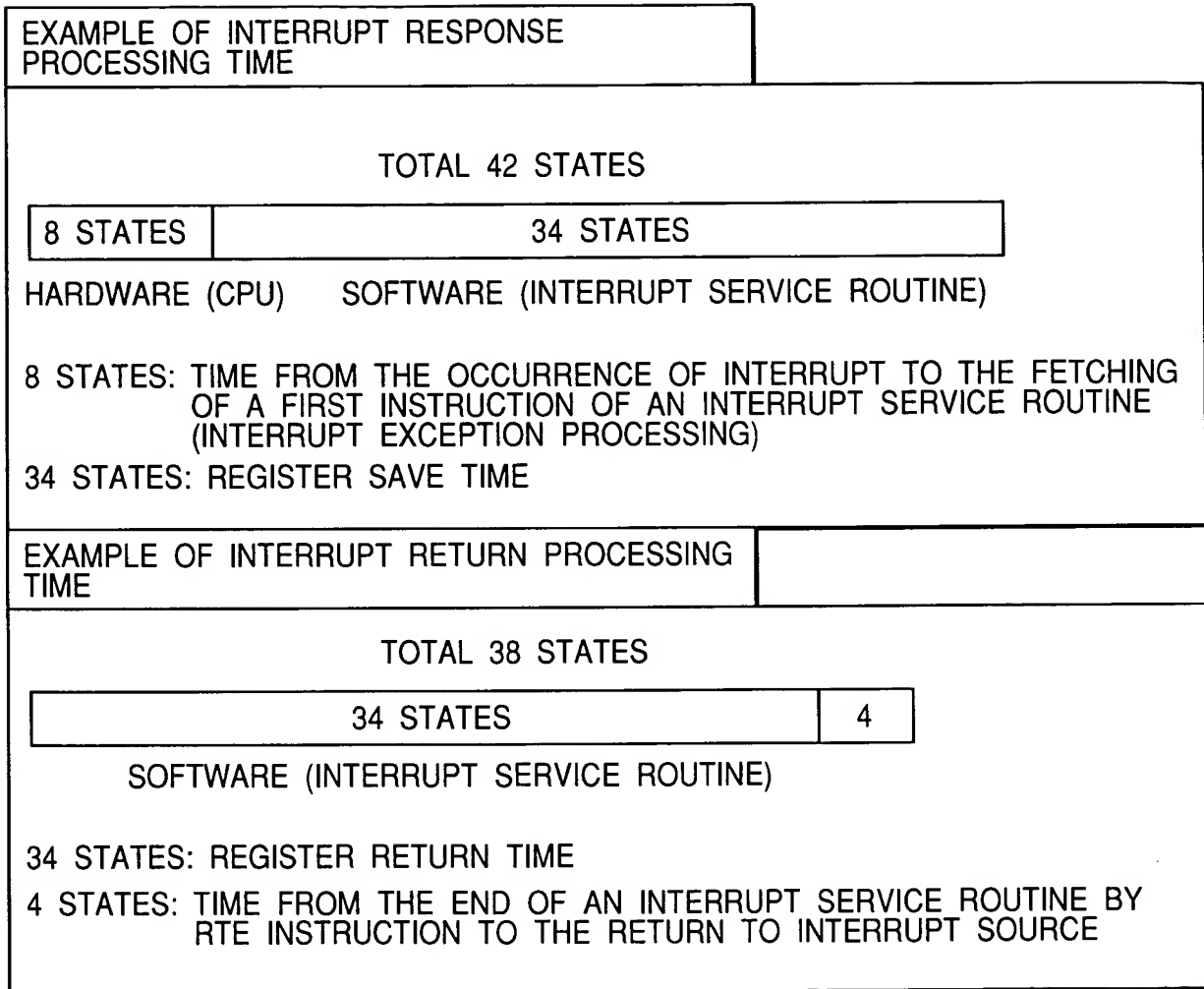
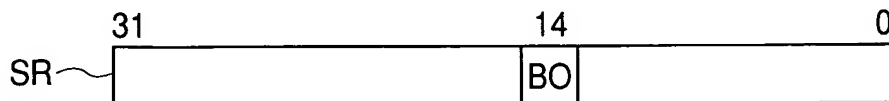
FIG. 7*FIG. 8*

FIG. 9

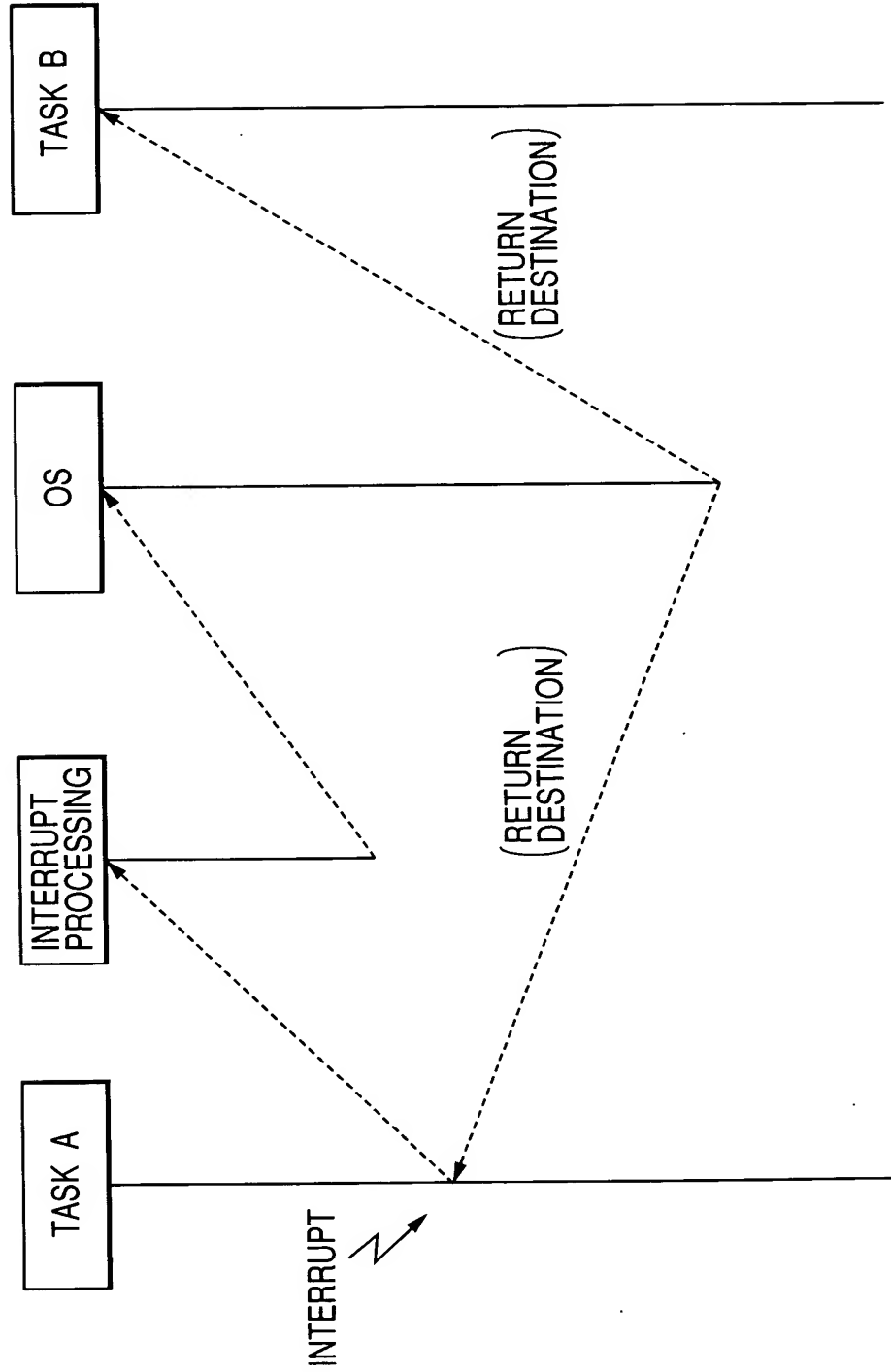


FIG. 10

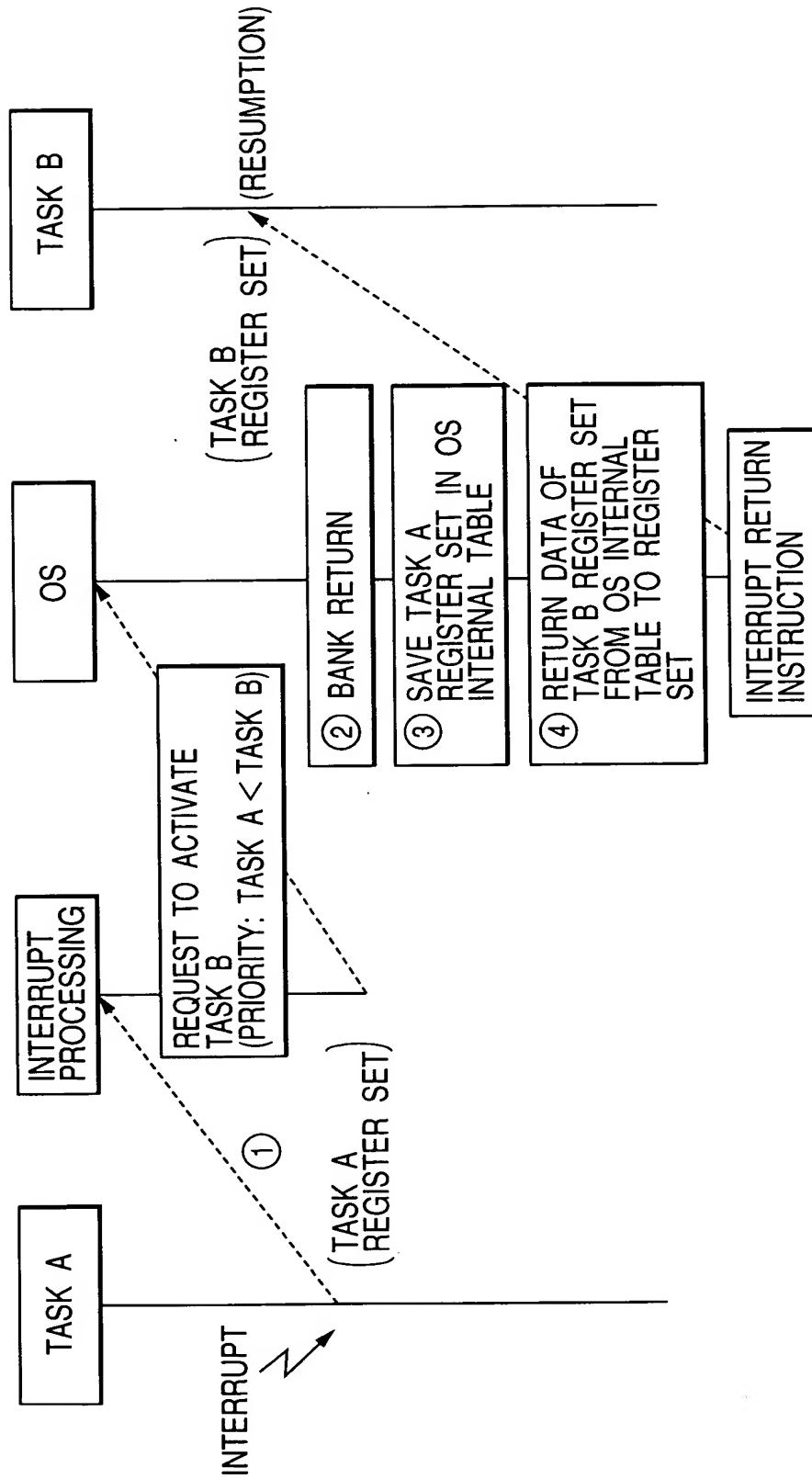


FIG. 11

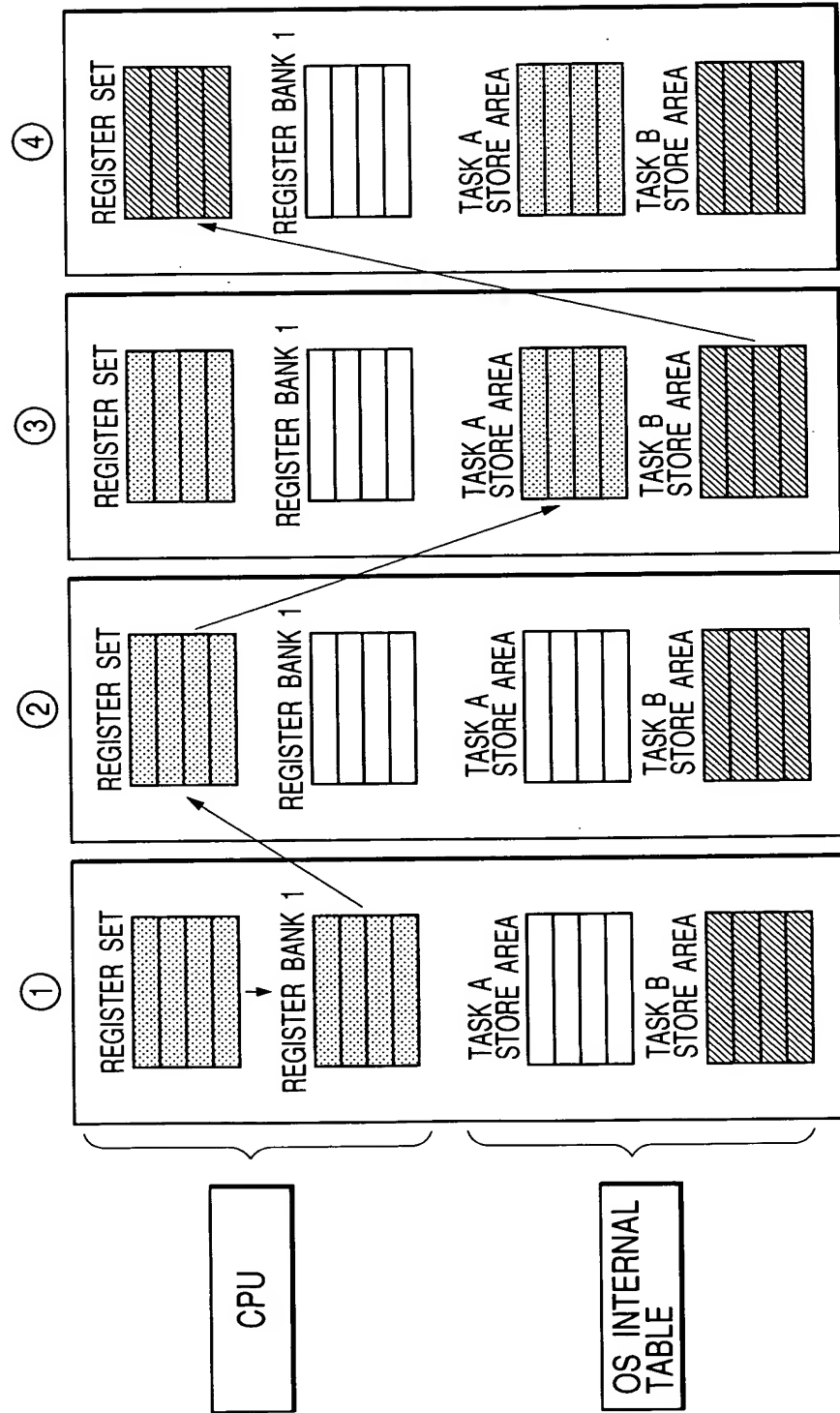
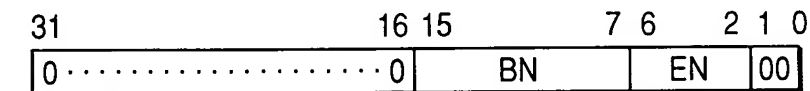


FIG. 12

MNEMONIC	OPERATION CONTENTS
LDBANK @Rm, R0	4-BYTE DATA FROM A REGISTER BANK ADDRESS INDICATED BY Rm IS TRANSFERRED TO R0
STBANK R0, @Rn	R0 IS TRANSFERRED TO A REGISTER BANK ADDRESS INDICATED BY Rn

FIG. 13

ADDRESS OF REGISTER BANK TRANSFER INSTRUCTION



REGISTER BANK (WHOLE)

000000000	BANK 0
000000001	BANK 1
000000010	BANK 2
000000011	BANK 3
	⋮
111111110	BANK N-2
111111111	BANK N-1

WHEN N = 512

REGISTER BANK (ONE BANK)

00000	R0
00001	R1
00010	R2
00011	R3
00100	R4
00101	R5
00110	R6
00111	R7
01000	R8
01001	R9
01010	R10
01011	R11
01100	R12
01101	R13
01110	R14
01111	MACH
10000	IVN
10001	PR
10010	GBR
10011	MACL

FOR 000000011

FOR 00110